REMARKS

Allowable Subject Matter

Claims 2, 5, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 2, 5, and 7, Applicants appreciate the Examiner's determination of allowable subject matter in the combination of claims 2, 5, and 7 with their base claims but respectfully submits that the independent claims also contain allowable subject matter in combination.

Claim Rejections - 35 USC §103

Claims 1 and 4 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ibnabdeljalil et al. (U.S. Patent No. 6,365,958, hereinafter "Ibnabdeljalil") in view of Mori (U.S. Patent No. 6,992,392, hereinafter "Mori").

Regarding claims 1 and 4, Applicants respectfully traverse the rejections since the Applicants claimed combinations, as exemplified in claim 1, includes limitations not taught or disclosed in Ibnabdeljalil in view of Mori of:

> "surrounding the guard ring with an oxide ring comprising a trench filled with an oxide."

The Examiner states:

> "Regarding claims 1 and 4, Ibnabdeljalil (e.g. fig. 7A-7c) show a method for creation of an ring 105 surrounding a guard ring 104 of a semiconductor die, comprising: providing a substrate 60 comprising semiconductor devices (col. 1/lls. 1-10) being accessible by points of electrical contact (e.g. contact 28 in fig. 2b; col. 5/lls. 20-30, 61-65; col. 6/lls. 44-50); provided in or over the substrate, the semiconductor devices comprising a semiconductor die 71 by being surrounded by a guard ring 104; creating at least one level of interconnect metal 104 (inner 104) with corresponding interconnect vias over the substrate aligned with the points of electrical contact; creating a *(sic)* surrounding the guard ring with a ring 105

comprising a trench filled 76, and located over the lateral surface area of the semiconductor die; and singulating the substrate into semiconductor die by sawing along sawing paths *(sic)* (col. 1/lls. 14-30)."

Applicants respectfully disagree. It is respectfully submitted that Ibnabdeljalil (e.g. fig. 7A-7C) does not teach or disclose surrounding the guard ring with an oxide ring comprising a trench filled with an oxide. Ibnabdeljalil does instead disclose a seal area having sacrificial structures comprising individual seal structures and a network of cross hatch pattern structures of metal lines forming walls of constant cross-section as taught in Ibnabdeljalil column 11, line 19, through column 12, line 24, which states:

"FIGS. 7A, 7B and 7C illustrate another embodiment of the present invention in simplified and schematic manner ... Between the chip data edge and the dicing street is an area of each chip, denoted by reference numbers comprising "c", which contains sacrificial structures according to the present invention ... the term "seal area" will be used.
... The cross sections through the individual seal structures 104 look the same in FIG. 7B as they do in FIG. 7C, since these structures are basically walls of constant cross section, surrounding the complete perimeter of the circuit chip. In contrast, the cross section of the network structures look different in FIG. 7B (reference number 105) compared to FIG. 7C ... The embodiment comprises a combination of sacrificial structures: A plurality of individual seal structures in addition to a network of cross hatch pattern strucutres.*(sic)* ... The combination of sacrificial structures has to fit into the seal areas 72c and 73c of FIGS. 7B and 7C. Consequently, their geometrical dimensions have to be appropriately as small as the dimensions of circuit elements. For instance, the width of metal lines 76 is typically in the range between 1 and 3 .mu.m, with a preferred width of 2 .mu.m, ... As can be seen from FIGS. 7B and 7C in combination with FIG. 7A, each set of sacrificial structures follows the respective longitudinal edges of the scribe lines in an approximately parallel manner. In addition, each set follows the respective data edges of the integrated circuit in an approximately parallel manner."[underline and deletions for clarity]

Applicants respectfully submit that element 105 of Ibnabdeljalil is not an oxide ring, but is instead a network of cross hatch pattern structures formed of metal lines 76.

The Examiner continues:

"Ibnabdeljalil does not teach that the ring 105 is made of oxide."

The Applicants respectfully agree. Applicants respectfully submit that element 105 of Ibnabdeljalil is not a ring, but is a seal area containing sacrificial metal structures, as shown above.

The Examiner further continues:

> "Nevertheless, Mori (e.g. fig. 5) teaches a method that includes a protection ring 22 made of oxide (col. 4/lls. 5-65). Also, this type of embodiment may prevent wiring deformation in addition to suppress negative effects of the of compression forces (col. 4/lls. 25-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the ring 105 disclosed by Ibnabdelijalil of oxide to prevent wiring deformation in addition to suppress negative effects of the of compression forces as taught by Mori."

Applicants respectfully disagree. Mori does not teach or disclose surrounding the guard ring comprising a trench filled with an oxide, but rather teaches and discloses a stress relieving dielectric layer, disposed on the base, patterned between the wiring layers as taught in column 4, lines 13-42, which states:

> "The stress relieving dielectric layers 22 having a specified pattern are disposed on the base 10 between the wiring layers 12 ... For example, according to the 0.13 .mu.m generation design rule, the minimum line width of metal wiring layers is 0.20 .mu.m, and the minimum gap is 0.22 .mu.m. By forming the stress relieving dielectric layers 22 according to such a rule, the stress relieving dielectric layers with miniature patterns can be formed, which can suppress the influence of compression forces of the planarization dielectric layer 26 that may act on the wiring layers 12 to a minimum level." [underline for clarity]

Applicants respectfully submit that the term "guard ring" does not appear in either Ibnabdelijalil or Mori, and Mori doesn't teach or suggest using an oxide in a trench, but rather teaches dielectric layers disposed on a base to suppress the compression forces of the planarization dielectric. It is known to those skilled in the art that oxide disposed on a base does not use a trench, as depicted in Mori figure 2. Applicants respectfully submit that with respect to claims 1 and 4, that taken as a whole, Ibnabdelijalil in view of Mori does not teach or suggest a method for creation of an oxide ring surrounding a guard ring of a semiconductor die, comprising: providing a substrate comprising semiconductor devices being accessible by points of electrical contact provided in or over the substrate, said semiconductor devices

comprising a semiconductor die by being surrounded by a guard ring, creating at least one level of interconnect metal with corresponding interconnect vias over the substrate aligned with said points of electrical contact, and surrounding the guard ring with an oxide ring comprising a trench filled with an oxide. Based on all of the above, it is respectfully submitted that claims 1 and 4 are allowable under 35 U.S.C. §103(a) as being patentable over Ibnabdelijalil in view of Mori because:

> "[T]he prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." **[bold** for clarity] *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

The Examiner rejected claims 4 and 6 under 35 U.S.C. §103(a) as being unpatentable over Ibnabdeljalil et al. (U.S. Patent No. 6,365,958, hereinafter "Ibnabdeljalil") in view of Mori (U.S. Patent No. 6,992,392, hereinafter "Mori") and further in view of Lee et al. (U.S. Patent No. 6,448,113, hereinafter "Lee").

Applicants believe that the Examiner intended to address claims 3 and 6, which are related to the use of Undoped Silicon Glass, rather than claim 4 which is addressed above. The Applicants further believe that the Examiner has an incorrect patent number for Lee et al. Applicants believe the correct patent number should be U.S. Patent No. 6,448,113, as detailed in the "Notice of References Cited".

Regarding claims 3 and 6, Applicants respectfully traverse the rejection since the Applicants' claimed combination includes the limitations of the independent claims 1 and 4 from which they respectively depend and include the limitation not disclosed in Ibnabdelijalil in view of Mori and further in view of Lee of:

"the oxide comprising Undoped Silicon Glass (USG)."

The Examiner states:

> "Regarding claims 4 and 6 -Ibnabdeljalil- in-view-of Mori teaches most aspects of the instant invention including a (*sic*) oxide ring made of silicon oxide but does not teach that the silicon oxide is an undoped silicon glass (USG)."

Applicants respectfully disagree. Applicants respectfully submit that Ibnabdeljalil teaches fabricating a seal area around the perimeter of the integrated circuit and does not mention having a guard ring or a trench filled with an oxide as shown above. While Mori teaches the use of a dielectric layer between metal layers, Mori does not teach or disclose using oxide in a trench as shown above. The Applicants do respectfully agree that neither cited art suggests or teaches the use of undoped silicon glass.

The Examiner further states:

> "Nevertheless, Lee teaches that silicon oxide can be produced as undoped silicon glass (col. 1/II. 67-col. 2/ll. 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the silicon oxide ring disclosed by Ibnabdeljalil in view of Mori of USG as suggested by Lee to provide be an enhanced structural stability."

Applicants respectfully disagree. Lee does not teach the oxide comprising undoped silicon glass, but instead teaches a silicon oxide as a combination of other silicon based oxides as taught in Lee column 1, line 67, through column 2, line 6, which states:

> "The interlayer dielectric films 26, 36, and 40 exposed on the sidewall of the fuse opening 50 are formed of silicon oxide, in particular, boron phosphorous silicate glass (BPSG), phosphorous silicate glass (PSG), spin on glass (SOG), tetra ethyl ortho silicate (TEOS), **and** undoped **silicate** glass (USG) which have an excellent step coverage, in order to reduce a large step difference between a cell array area and a peripheral circuit area." [bold and underline for clarity]

Applicants respectfully submit that the element "undoped silicon glass" does not appear within Lee. Applicants further submit that with respect to claims 3 and 6, that taken as a whole, Ibnabdelijalil in view of Mori and further in view of Lee does not teach or suggest a method for creation of an oxide ring surrounding a guard ring of a semiconductor die, comprising: providing a substrate comprising semiconductor devices being accessible by points of electrical contact provided in or over the substrate, said semiconductor devices comprising a semiconductor die by being surrounded by a guard ring, creating at least one level of interconnect metal with corresponding interconnect vias over the substrate aligned with said points of electrical contact, and surrounding the guard ring with an oxide ring comprising a trench filled with an oxide, wherein the oxide is undoped silicon glass. Based on all of the above, it is respectfully submitted that claims 3 and 6 are allowable under 35 U.S.C.

§103(a) as being patentable over Ibnabdelijalil in view of Mori and in further view of Lee because of the holding in *In re* Vaeck, *supra*.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1-7 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

William D. Zahrt II
Registration No. 26,070

The Law Offices of Mikio Ishimaru
333 W. El Camino Real, Suite #330
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881
Date: October 2, 2006